Electronics Image Stabilization, EIS

1. REVISION HISTORY

Revision Date	Revision	Description
01/28/2014	1.0	Initial Release
08/19/2014	2.0	Added additional implementations / merged app notes

2. PURPOSE

Electronic Image Stabilization is a jitter compensation method for a video stream. The source of the jitter is typically natural hand motion, which is detected by a gyroscope and sent to an ISP (image signal processor). The ISP uses the direction and displacement of the hand movement provided by the gyro to crop the target video frame (for example 1080 x 1920 full HD) from a location in opposite direction from a high-resolution image sensor on the next frame to compensate for the jitter. A key element in successful compensation is synchronizing the gyro samples for a given frame to the exact frame it was for in a video stream. The synchronization often gets more complicated as ISPs vary the frame rate due to system overhead and lighting condition to maintain best exposure.

InvenSense gyroscopes, optimized for image stabilization, employ a method to ease such synchronization between gyro samples using a FSYNC (Frame Sync) pin and FIFO that stores tagged samples for each frame. This application note describes the use of ITG-3521, a 3-axis gyroscope optimized for image stabilization with very low noise and high sensitivity for EIS using FSYNC.

There is also a mode during which gyro data can be read directly from gyro sensor register (no need for FSYNC and FIFO) using interrupt (section 7.3).

3. RELATED DOCUMENTS

The following documents are recommended to fully understand the products and systems described in this application note:

- InvenSense ITG-3521 Datasheet
- InvenSense ITG-3521 Register Map

InvenSense Inc.
1745 Technology Drive, San Jose, CA 95110 U.S.A
+1(408) 988–7339
www.invensense.com

Document Number: AN-xxxxxx
Revision: Draft, 1.0
Release Date: 01/28/14

CONTENTS

4. IMPLEMENTATIONS

There are several ways to implement an EIS enabled system. Each implementation includes various tradeoffs. This application note will describe three implementations:

- FIFO + FSYNC + INT
- FIFO + FSYNC
- Gyro Data Register + INT

• FIFO + FSYNC + INT

The FIFO + FSYNC + INT method utilizes the gyroscope sensor FIFO to buffer sensor data and FSYNC data internally and generates an interrupt to the AP when a full video frame is complete. This allows the application processor to be interrupt driven and lowers the overhead in the application processor (or video processor) by concatenating the FSYNC with the gyroscope sensor data.

• FIFO + FSYNC

The FIFO + FSYNC method is similar to the method above with the only difference being a polled implementation instead of an interrupt driven implementation.

• GYRO DATA REGISTER + INT

The register + INT method bypasses the sensor FIFO buffer and FSYNC concatenation and instead generates an interrupt when sensor data is available and the application or image processor takes responsibility for all of the synchronization.

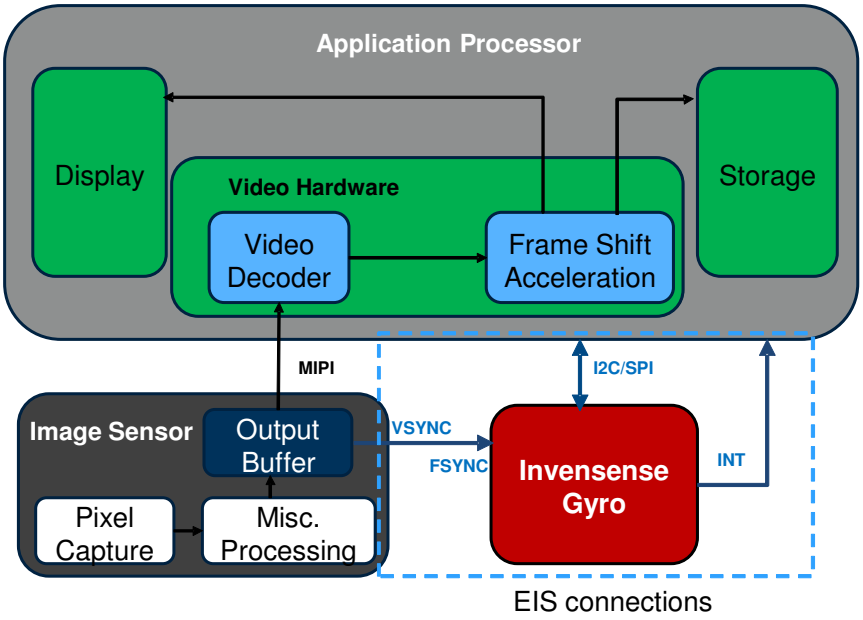
• BUS SPEED / TYPE

The ITG-3521 supports both an I2C and SPI interconnect to the applications processor. However, it is critical to understand the nature of the data rate and data rates to determine the correct implementation for a given implementation. Sampling rates above 1 KHz will require the use of the SPI interconnect to avoid bus overflow.

5. EIS SYSTEM BLOCK DIAGRAMS

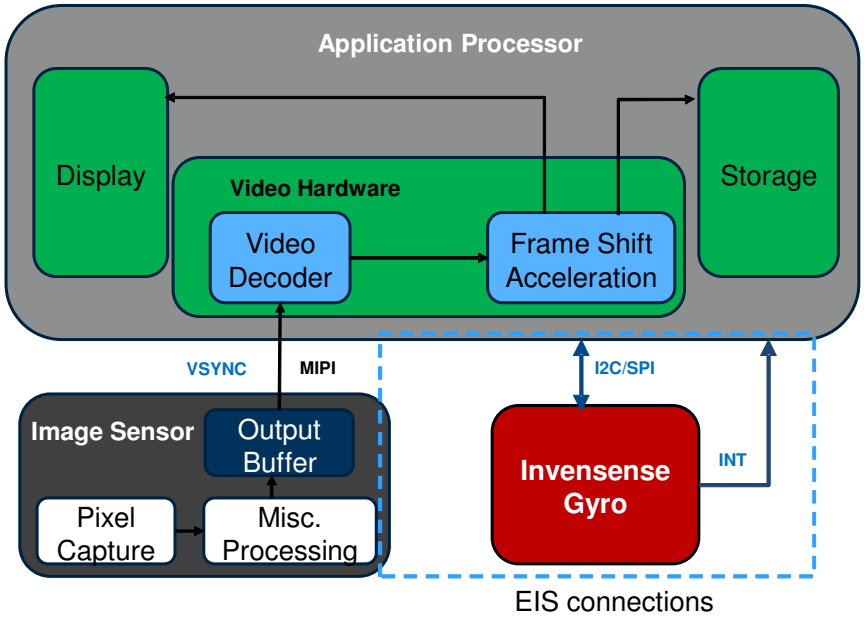
- ### FIFO + FSYNC + INT / FIFO + FSYNC

For either the FIFO + FSYNC + INT method or the FIFO + FSYNC method, the block diagram below shows how Invensense's ITG-3521 connects to the image sensor and Application Processor, AP. In the case of FIFO + FSYNC the INT line is not connected. The VSYNC signal generated by an image sensor connects to the FSYNC input pin of ITG-3521. In the INT implementation, this signal is used to trigger an interrupt signal to the AP, letting it know the gyro data for a complete frame is ready to be read from the ITG-3521 FIFO. The data is then transferred through I2C/SPI bus to the AP.



- ***GYRO DATA REGISTER + INT***

For either the Register + INT method, the block diagram below shows how Invensense's ITG-3521 connects to the Application Processor, AP. In this case, the AP is responsible for the synchronization of the VSYNC and gyroscope data. The VSYNC is part of the MIPI interface from the image sensor. The gyroscope connects to the AP via the I2C/SPI interface and generates an interrupt when new data is available.



6. TIMING DIAGRAM OF FSYNC (FIFO+FSYNC+INT / FIFO+FSYNC)

The rising edge of VSYNC indicates the Start of the Frame, SOF. Let us consider an example. If the frame rate is 30 frames per second, the frame length is going to be 33.333 ms as shown in Figure 1. The sampling rate for the ITG-3521 data is set to 1 kHz in this example. With this sampling rate at each frame length, we would have 33.333 frames or 33 frames for simplicity. The gyro data for all three axes, X, Y, and Z can be stored in FIFO through the register setting, explained in section 7.1. The value of FSYNC signal can be sampled and stored as LSB value in any of the Xout, Yout, or Zout data registers. In the example below (Figure 1), we are storing the sampled value of the FSYNC signal in Zout[0]. When the value of the FSYNC is low, the value "0" is stored in Zout[0] and when FSYNC is high, the value "1" is stored in Zout[0]. This value can be stored in Xout[0] or Yout[0] as well. When AP reads out the FIFO upon receiving an interrupt, all the read data with LSB equaling "0" is considered generated for a single frame. In the example below, the AP reads the FIFO content which has ~30 sample sets of gyro outputs corresponding to Xout[15:0], Yout[15:0], Zout[15:1], and Zout[0] = 0 for 30 images in a single frame. We will discuss how to set up the internal registers of ITG-3521 to enable this operation in the next section. Please note that in FIFO+FSYNC there is no need for an interrupt signal as shown in Figure 1 and the AP manages reading the FIFO data. Additionally the sampled FSYNC signal will lag the true FSYNC input by up to one ODR period.

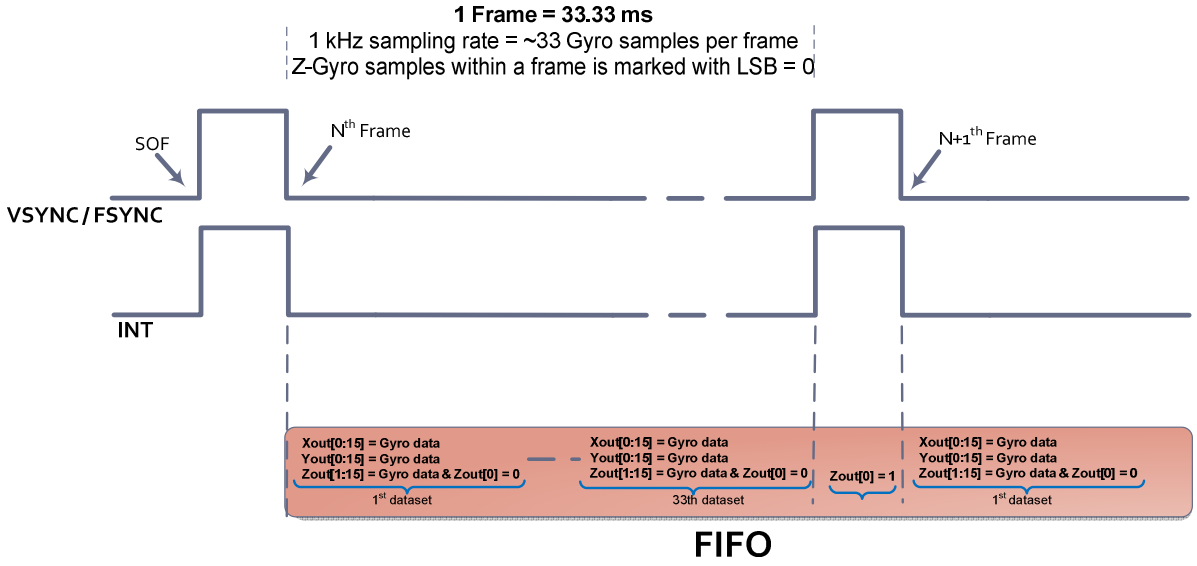


Figure 1. Timing Diagram

7. RECOMMENDED REGISTERS VALUES

As mentioned earlier there are three methods to read the ITG-3521 data.
Section 7.1 explains the settings that are in common for all the three methods. Section 7.2 explains the FIFO+FSYNC+INT/FIFO+FSYNC methods and Section 7.3 discusses the gyro data register method with interrupt.

• COMMON SETTINGS FOR ALL THREE METHODS

7..1. FULL-SCALE RANGE (FSR) SETTING

- **Register 0x1B, GYRO_CONFIG**

  FS_SEL (GYRO_CONFIG [3:4]): For EIS applications using ITG-3521, these bits should be set to "11" to achieve recommended full-scale range (FSR) of ±250 dps, providing the widest range for EIS.

7..2. LOW-PASS FILTER (DLPF) SETTING

- **Register 0x1B, GYRO_CONFIG and 0x1A, CONFIG**

  The first setting at 1Khz ODR and 184Hz LPF will work for most applications. Higher ODR and LPF setting maybe selected to achieve the precision that the target application may require.

Sampling Rate	DLPF BW	FCHOICE_B (GYRO_CONFIG[1:0])	DLPF_CFG (CONFIG [2:0])
1 kHz	184 Hz	00	001

8 kHz	250 Hz	00	000
32 kHz	8.8 kHz	x1	xxx
32 kHz	3.6 kHz	10	xxx

7..3. OUTPUT DATA RATE (ODR) SETTING

- **Register 0x19, SMPLRT_DIV**

  SMPLRT_DIV[7:0]: The gyroscope output rate can be divided by value of this register to generate a reduced sample rate. Recommend sample rate is 1 kHz with a digital low-pass filter (DLPF) setting of 184 Hz. This configuration is achieved by setting proper bits at DLPF_CFG[0:2] = 001 (register 0x1A) and FCHOICE_B[1:0] = 00 (register 0x1B).
  With above setting, the SMPLRT_DIV divider is bypassed.

- ***FIFO + FSYNC + INT / FIFO + FSYNC METHODS***

In these methods, the tagged gyro data is stored in FIFO. The FSYNC is used to tag the data based on the logic level of the signal (V-Sync) connected to FSYNC pin of ITG-3521. The V-Sync is signal provided by image sensors to indicate the start or end of a video frame. The value of the signal connected to FSYNC can be sampled and stored as the LSB value in any of Xout, Yout, or Zout data registers. Checking the tags by AP provides an extra level of data validation that the read out gyro data corresponds to an active V-sync signal. In the FIFO+FSYNC method, the FIFO has to be read by the AP often enough to prevent overflowing of the data. Based on 512 byte FIFO available in ITG-3521, the read out intervals are indicated below:

Sampling Rate	FIFO Reading Interval	# of FIFO reads / second
1 kHz	85 ms	12
8 kHz	10.625 ms	93
32 kHz	2.66 ms	375

- **FIFO AND FSYNC SETTINGS FOR BOTH FIFO+FSYNC+INT AND FIFO+FSYNC METHODS**

- **Register 0x1A, CONFIG**

  FIFO_MODE (CONFIG [6]): By setting this bit to “0,” additional writes will be written to the FIFO, replacing the oldest data.

  EXT_SYNC_SET (CONFIG [5:3]): An external signal connected to the FSYNC pin can be sampled by configuring these bits.

  Signal changes to the FSYNC pin are latched so that short strobes may be captured. The latched FSYNC signal will be sampled at the sampling rate defined in registers 0x19 and 0x1A (1 kHz). After sampling, the latch will reset to the current FSYNC signal state. The sampled value will be reported in place of the least significant bit in a sensor data register determined by the value of EXT_SYNC_SET according to the following table.

EXT_SYNC_SET	FSYNC Bit Location
2 (“010”)	GYRO_XOUT_L[0]
3 (“011”)	GYRO_YOUT_L[0]
4 (“100”)	GYRO_ZOUT_L[0]

Figure 2.

- **Register 0x6A, USER_CTRL**

  FIFO_EN (USER_CTRL[6]): Setting this bit to “1” enables FIFO operations.

- **Register 0x23, FIFO_EN**

  XG _FIFO_EN (FIFO_EN[6]): By setting this bit to “1”, the X Gyro data will be loaded into the FIFO buffer.

  YG _FIFO_EN (FIFO_EN[5]): By setting this bit to “1”, the Y Gyro data will be loaded into the FIFO buffer.

ZG _FIFO_EN (FIFO_EN[4]): By setting this bit to “1”, the Z Gyro data will be loaded into the FIFO buffer.

They are sampled at the sample rate defined in 0x19 and 0x1A registers.

- **Register 0x74, FIFO Read Write**

  FIFO_DATA (FIFO_R_W [0:7]): The content of the FIFO can be read from this register.

- **INTERRUPT SETTING FOR FSYNC+FIFO+INT MEHTOD**

  - **Register 0x37, INT_PIN_CFG**

    INT_OPEN (INT_PIN_CFG [6])**:** Setting the value of this bit to “0” means INT pin is configured as push-pull. Setting it to “1” means the INT pin is open drain.

    LATCH_INT_EN (INT_PIN_CFG [5])**:** This bit has to be set to “0” to allow INT pin to emit a 50 µs long pulse.

    INT_RD_CLEAR (INT_PIN_CFG [4])**:** This bit has to be set to “0” to enable clearing the INT only by reading INT_STATUS of register 0x3A.

    FSYNC_INT_LEVEL (INT_PIN_CFG [3]): When this bit is equal to “0”, the logic level for the FSYNC pin (when used as an interrupt to the host processor) is active high. When this bit is equal to “1”, the logic level for the FSYNC pin (when used as an interrupt to the host processor) is active low.

    FSYNC_INT_MODE_EN (INT_PIN_CFG [2])**:** When this bit is equal to 1, the FSYNC pin will trigger an interrupt when it transitions to the level specified by FSYNC_INT_LEVEL. When a FSYNC interrupt is triggered, the FSYNC_INT bit in Register 0x3A will be set to 1. An interrupt is sent to the host processor if the FSYNC interrupt is enabled by the FSYNC_INT_EN bit in Register 0x38.

  - **Register 0x38, INT_ENABLE**

    FSYNC_INT_EN (INT_ENABLE [3]): This bit has to be set to “1” to enable the FSYNC pin to be used as an interrupt to the host processor.

    FIFO_OFLOW_EN (INT_ENABLE [4]): This bit should be set to “0”.

    DATA_RDY_EN (INT_ENABLE [0]): This bit should be set to “0”.

  - **Register 0x3A, INT_STATUS**

    FSYNC_INT (INT_ENABLE [3]): This bit automatically sets to 1 when an FSYNC interrupt has been generated. The bit clears to 0 after the registers have been read.

    FIFO_OFLOW_INT (INT_STATUS [4]): This bit should be set to “0”.

    DATA_RDY_INT (INT_STATUS [0]): This bit should be set to “0”.

- ***GYRO DATA REGISTER + INTERRUPT METHOD***
- **Register 0x6A, USER_CTRL**

  I2C_IF_DIS (USER_CTRL[4]): This bit has to be set to “1” to enable SPI operations.

- **Register 0x37, INT_PIN_CFG**

  INT_OPEN (INT_PIN_CFG [6])**:** Setting the value of this bit to “0” means the INT pin is configured as push-pull. Setting it to “1” means the INT pin is open drain.

LATCH_INT_EN (INT_PIN_CFG [5])**:** This bit has to be set to "0" to allow INT pin to emit a 50 µs long pulse when sampling at 1 kHz or 8 kHz and 16 µs long pulse when sampling at 32 kHz.

INT_RD_CLEAR (INT_PIN_CFG [4])**:** This bit has to be set to "0" to enable clearing the INT only by reading INT_STATUS of register 0x3A.

- **Register 0x38, INT_ENABLE**

  DATA_RDY_EN (INT_ENABLE [0]): This bit should be set to "1". The Data Ready interrupt occurs when all the sensor registers have been written with the latest gyro sensor data

  FSYNC_INT_EN (INT_ENABLE [3]): This bit has to be set to "0" to disable the FSYNC signal to generate an interrupt.

  FIFO_OFLOW_EN (INT_ENABLE [4]): This bit should be set to "0".

- **Register 0x3A, INT_STATUS**

  DATA_RDY_INT (INT_STATUS [0]): This bit automatically sets to 1 when a Data Ready interrupt has been generated. The bit clears to 0 after the registers have been read.

  FSYNC_INT (INT_ENABLE [3]): This bit should be set to "0"

  FIFO_OFLOW_INT (INT_STATUS [4]): This bit should be set to "0".

8. REGISTER SUMMARY

- *FIFO + FSYNC + INT*

FIFO + FSYNC + INT Method – Recommended Register Settings

ADDR (HEX)	NAME	SERIAL IF / VALUE	BIT 7	6	5	4	3	2	1	0
19	SMPLRT_DIV	R/W	SMPLRT_DIV[7:0]							
		Recommended Value	0	0	0	0	0	0	0	0
1A	CONFIG	R/W	-	FIFO_MODE	EXT_SYNC_SET[2:0]			DLPF_CFG[2:0]		
		FIFO overwrites allowed FSYNC stored in Zout(0) DLPF = 184 Hz and 1Khz sample rate	-	0	1	0	0	0	0	1
1B	GYRO_CONFIG	R/W	-	-	-	FS_SEL[1:0]		-	FCHOICE_B[1:0]	
		FSR = +/- 250 dps	-	-	-	1	1	-	0	0
23	FIFO_EN	R/W	TEMP_FIFO_EN	XG_FIFO_EN	YG_FIFO_EN	ZG_FIFO_EN	-	-	-	-
		X, Y and Z gyro data written to FIFO	0	1	1	1	-	-	-	-
37	INT_PIN_CFG	R/W	INT_LEVEL	INT_OPEN	LATCH_INT_EN	INT_RD_CLEAR	FSYNC_INT_LEVEL	FSYNC_INT_MODE_EN	-	-
		INT Level is active high, open drain, pulse mode	1	1	0	0	1	1	-	-
38	INT_ENABLE	R/W	-	-	-	FIFO_OFLOW_EN	FSYNC_INT_EN	-	-	DATA_RDY_EN
		FSYNC to trigger an interrupt to AP	-	-	-	0	1	-	-	0
3A	INT_STATUS	R/W	-	-	-	FIFO_OFLOW_INT	FSYNC_INT	-	-	DATA_RDY_INT
		Generate INT on FSYNC Clear INT status on read	-	-	-	0	1	-	-	0
6A	USER_CTRL	R/W	-	FIFO_EN	-	I2C_IF_DIS	-	-	-	-
		Enable FIFO Enable I2C	-	1	-	0	-	-	-	-

- ***FIFO + FSYNC***

FIFO + FSYNC Method – Recommended Register Settings											
ADDR (HEX)	NAME	SERIAL IF / VALUE	BIT								
			7	6	5	4	3	2	1	0	
19	SMPLRT_DIV	R/W	SMPLRT_DIV[7:0]								
		Recommended Value	0	0	0	0	0	0	0	0	
1A	CONFIG	R/W	-	FIFO_MODE	EXT_SYNC_SET[2:0]			DLPF_CFG[2:0]			
		FIFO overwrites allowed FSYNC stored in Zout(0) DLPF = 184 Hz and 1 Khz sample rate	-	0	1	0	0	0	0	1	
1B	GYRO_CONFIG	R/W	-	-	-	FS_SEL[1:0]		-	FCHOICE_B[1:0]		
		FSR = +/- 250 dps	-	-	-	1	1	-	0	0	
23	FIFO_EN	R/W	TEMP_FIFO_EN	XG_FIFO_EN	YG_FIFO_EN	ZG_FIFO_EN	-	-	-	-	
		X, Y and Z gyro data written to FIFO	0	1	1	1	-	-	-	-	
37	INT_PIN_CFG	R/W	INT_LEVEL	INT_OPEN	LATCH_INT_EN	INT_RD_CLEAR	FSYNC_INT_LEVEL	FSYNC_INT_MODE_EN	-	-	
		No INT	0	0	0	0	1	0	-	-	
38	INT_ENABLE	R/W	-	-	-	FIFO_OFLOW_EN	FSYNC_INT_EN	-	-	DATA_RDY_EN	
		FSYNC to trigger an interrupt to AP	-	-	-	0	0	-	-	0	
3A	INT_STATUS	R/W	-	-	-	FIFO_OFLOW_INT	FSYNC_INT	-	-	DATA_RDY_INT	
		Generate INT on FSYNC Clear INT status on read	-	-	-	0	0	-	-	0	
6A	USER_CTRL	R/W	-	FIFO_EN	-	I2C_IF_DIS	-	-	-	-	
		Enable FIFO Enable I2C	-	1	-	0	-	-	-	-	

- ***REGISTER + INT***

REGISTER + INT Method – Recommended Register Settings											
ADDR (HEX)	NAME	SERIAL IF / VALUE	BIT								
			7	6	5	4	3	2	1	0	
19	SMPLRT_DIV	R/W	SMPLRT_DIV[7:0]								
		Recommended Value	0	0	0	0	0	0	0	0	
1A	CONFIG	R/W	-	FIFO_MODE	EXT_SYNC_SET[2:0]			DLPF_CFG[2:0]			
		FIFO overwrites allowed FSYNC stored in Zout(0) DLPF = 184 Hz and 1Khz sample rate	-	0	1	0	0	0	0	1	
1B	GYRO_CONFIG	R/W	-	-	-	FS_SEL[1:0]		-	FCHOICE_B[1:0]		
		FSR = +/- 250 dps	-	-	-	1	1	-	0	0	
23	FIFO_EN	R/W	TEMP_FIFO_EN	XG_FIFO_EN	YG_FIFO_EN	ZG_FIFO_EN	-	-	-	-	
		X, Y and Z gyro data written to FIFO	0	1	1	1	-	-	-	-	
37	INT_PIN_CFG	R/W	INT_LEVEL	INT_OPEN	LATCH_INT_EN	INT_RD_CLEAR	FSYNC_INT_LEVEL	FSYNC_INT_MODE_EN	-	-	
		INT Level is active high, open drain, pulse mode	1	1	0	0	1	1	-	-	
38	INT_ENABLE	R/W	-	-	-	FIFO_OFLOW_EN	FSYNC_INT_EN	-	-	DATA_RDY_EN	
		FSYNC to trigger an interrupt to AP	-	-	-	0	0	-	-	1	
3A	INT_STATUS	R/W	-	-	-	FIFO_OFLOW_INT	FSYNC_INT	-	-	DATA_RDY_INT	
		Generate INT on FSYNC Clear INT status on read	-	-	-	0	0	-	-	1	
6A	USER_CTRL	R/W	-	FIFO_EN	-	I2C_IF_DIS	-	-	-	-	
		Disable FIFO Enable ISPI	-	0	-	1	-	-	-	-	

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